Solutions

Problem 1: ***Technology Boosters***

In order to enable the scaling of CMOS into the nanometer regime and keep a high performance, a series of so called technology boosters (by definition, a technology innovation that improves some of the device performance in static and/or dynamic operation) are applied, such as strain, high-k dielectrics, metal gate, new channel replacement materials, etc. Select the correct statements concerning such performance boosters.

1. **Tensile strain** improves the mobility of both electrons and holes and, therefore, is a performance booster for both n- and p-type channel MOSFETs.
2. **A Ge (germanium) channel** in a p-type MOSFET can be considered a technology booster. Explain why or why not.
3. **A InAs channel** in a n-type MOSFET can be considered a technology booster. Explain why or why not.
4. The **high-k dielectric** allows for having the same capacitance of the gate with a thicker dielectric layer (compared with SiO2) for the same capacitance, and reduces the gate leakage current.
5. The **mobility of electrons** in strained channels can be boosted by more than 15%, depending of the amount of applied tensile strain.
6. The **subthreshold swing** of a MOSFET can be improved by the application of **strain**.
7. The Ioff current cannot be influenced by strain.
8. A **very thin channel in a SOI MOSFET can be considered a technology booster** (i.e. improves some of the performance aspects at same dimensions of the transistor).
9. The **multi-gate transistor** architectures are not technology boosters.
10. **Scaling of channel dimensions** is in itself a technology booster for CMOS.
11. Using a **carbon nanotube with higher carrier mobility** instead of a silicon channel in a gate-all-around nanowire FET is a technology booster.
12. The use of 2D-material channels in MOSFET is NOT a technology booster. Motivate with physics arguments of bandgap and mobility why this is true or not true.

<u>Problem 2</u>: Tunnel FET as Steep Slope Switch basics

The Tunnel FET is a gated p-i-n diode device operating in reversed bias regime and exploiting quantum-mechanical band-to-band tunneling. Select the correct properties of this steep slope device:

1. Dennard scaling rules applies to both MOSFETs and Tunnel FETs.
2. A Tunnel FET with InAs source and same geometry and dimensions as an all-silicon Tunnel FET has a lower Ion current.
3. An optimized Tunnel FET (high Ion and low Ioff) should be asymmetrical from the point of drain and source materials because an identical band-gap at source and drain can never optimize both Ion and Ioff.
4. The temperature dependence trend of subthreshold characteristics of Tunnel FET is very similar to the one of MOSFETs made of same semiconductor material; the subthreshold slope degrades with the temperature increase.
5. The quantum- mechanical tunneling effec exploited Tunnel FETs involves probability calculations for electrons to tunnel through a thin energy barrier.
6. Carrier mobility plays a key role in the transport characteristics of Tunnel FETs. Therefore materials with higher carrier mobility like III-V and Ge are suitable for these devices.
7. The effect of dimension (gate length, for instance) variability is expected to be quasi-identical on the Id-Vg and Id-Vd characteristics of Tunnel FETs and MOSFETs (consider how these characteristics change when the channel length is divided by a factor of x2, for instance).
8. The Electron-Hole Bilayer Tunnel FET is a Density of States switch that can achieve a steeper transition between off and on than a conventional Tunnel FET because the gate-controlled electrostatic field and the tunneling paths are aligned.
9. Tunnel FET exploits a discrete charge conduction principle (electrons tunnel one by one from the conduction to the valence band).
10. Tunnel FET can be scaled more aggressively that MOSFET because they have no short channel effects.

<u>Problem 3</u>: Trap-assisted tunneling effect, digital, analog, sensor and other applications of Tunnel FETs.

<u>Select the correct statements</u> about the Tunnel FETs from the list below:

1. Trap-Assisted Tunneling (TAT) is a phenomenon that depends on the *density of electrically-active traps* at both the oxide-to-channel interface and at the tunneling junctions. These densities of traps should be lower than 10^{12} $eV^{-1}cm^{-2}$ to have a good tunnel FET.
2. Trap-Assisted Tunneling (TAT) is a phenomenon that does not depends on temperature but only on the energy levels of traps.
3. Trap-Assisted Tunneling (TAT) is cancelled when the temperature is increasing.
4. The steep-slope of Tunnel FETs is normally steeper at higher levels of currents.
5. At low voltage and low current levels Tunnel FETs can offer higher analog amplification than CMOS. Support your answer with an approximate calculation of gm/Id limit at 300K in MOSFETs and compare it with what a Tunnel FET with a slope of 10mV/decade at 300K can achieve as gm/Id.
6. Tunnel FET can be used to design more energy efficient hybrid CMOS-TFET multi-core processor architecture. The computing tasks assigned to Tunnel FETs are the ones requiring high-performance (HP) specifications.
7. Leakage, Ioff, current of Tunnel FETs decreases at cryogenic (sub-77K) temperatures.
8. A charge sensor exploiting a tunnel FET operated in the sub-Vth region of Id-VG characteristics would offer a better current sensitivity to an elementary charge variation on the device gate.
9. Tunnel FET otput characteristics do saturate by pinch-off, like in MOSFETs. In case you disagree with this statement, what do you think is the saturation mechanisms of Id-Vd of tunnel FETs.
10. Tunnel FETs cannot be used to build 1T (one transistor) Active Pixel Sensors for imagers (optical sensing) because of their too small off-currents.